16.7 A 200dB Dynamic Range Iris-less CMOS Image Sensor with Lateral Overflow Integration Capacitor using Hybrid Voltage and Current Readout Operation

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In order to realize the ultimate performance image-sensing device, an enhanced dynamic range is required in addition to high sensitivity, high SNR and high resolution. Several recent papers have described methods for extending dynamic range (DR); such as, multiple exposures in a frame [1], logarithmic compression [2], a combination of linear and logarithmic responses [3] and a lateral overflow integration capacitor [4, 5]. These approaches have improved the DRs, but they are only 100 to 140dB of DRs. This paper describes a CMOS image sensor with over 200dB DR. The sensor features a hybrid readout operation; a voltage-readout operation based on the lateral overflow integration capacitor in the pixel and a current-readout operation based on current amplification and logarithmic compression.

Figure 16.7.1 shows the schematic diagram of a pixel. The pixel circuit consists of a fully depleted photodiode (PD), a transfer switch (T), a floating diffusion to convert the charge to a voltage (FD), a reset switch (R), a source follower amplifier (SF), a row select switch (X), an overflow photoelectron integration capacitor (CS), a connection switch between FD and CS (S), another transfer switch (T'), current mirror circuits amplifying the photocurrent from the PD (CM1, CM2), a reference current source (I_{REF}) and another row select switch (X1'). The column line component consists of a current source driven by the voltage readout operation (I_{Vol}) and a current readout circuit of the current readout operation, which includes the current mirror comprising CM3 and CM4, a common-gate transistor (X2') and a logarithmic compression circuit (LOG), in each column.

The voltage readout circuit with a lateral overflow integration capacitor in the pixel is the same as described in the previous paper [5] and leads to an extension of the DR keeping a high sensitivity and a high SNR without losing the overflow charge from the PD. The current readout circuit achieves further extension of the DR on the bright end of the range by reading out the logarithmic compression voltage of the photocurrent amplified in each pixel and column.

Figure 16.7.2 shows the timing diagram of the pixel circuits. The voltage readout operation follows the same timing diagram as described in the previous paper [5] and, in addition, incorporates the electrical shutter operation. During the integration period (t_3), the signal charges are integrated by the PD until it reaches saturation, then the overflow charges are integrated at FD+CS via switches T and S. This operation enables the overflow charges from the PD to be utilized for the signal. After the integration (t_4), the charges distributed to the FD are readout as the noise $N1$ by turning the switch S off. The signal charges are transferred from the PD to the FD by turning the switch T on (t_5) and readout as the signal $S1 + N1$. The signal charges at the PD are fully transferred to the FD+CS by turning the switch S on (t_6) and then readout as the signal $S2 + N2$. The high tolerance of the signal $S2$ for the dark current shot noise and the reset noise is achieved by the mixture of the signal charges. The FD+CS is reset by turning the switches T and R on (t_1') and the reset noise $N2$' is readout by turning the switches R and T off (t_2'). The noise $N2$' includes the fixed-pattern noise caused by the variation of the threshold voltage of the SF.

In the voltage readout operation, the signals $N1$, $S1 + N1$, $N2$' and $S2 + N2$ are readout from each pixel. The noise subtractions $(S1 + N1) - N1$ and $(S2 + N2) - N2$' are performed by the on-chip noise cancellation circuit. Either the noise-subtracted signal $S1$ or signal $S2$ is selected by the pixel as compared with the reference voltage level. Then the DR-extended image is reproduced by the composite signal with linear response from low light to very bright light.

The current readout operation consists of two phases, one is the reference-current readout and the other is the reference-current plus signal-current readout. The reference-current readout is performed by turning the switches R, S, T, and X1' on, and T' and X off (t_{1i}), applying V_{REF} to the gate of the transistor that produces I_{REF}, and keeping the reference current. The reference current is amplified by the pixel- and column-current mirror circuits and finally converted to the logarithmic compressed reference voltage Ni. Then the photocurrent at the PD and the reference current are readout from the same path by turning the switches R and T off and the switch T' on (t_{2i}), and the signal voltage superimposed on the reference voltage $Si + Ni$ is obtained. After that, the signal Si is readout by subtracting Ni from $Si + Ni$ through the on-chip noise cancellation circuit. Even in the current readout operation, the variation of the amplification by pixel and column is cancelled by this method.

Figure 16.7.3 shows the sensor block diagram. Assuming the use of a simplified optical lens and a sensor control system, the image sensor is designed as a relatively small number of pixels (64H×64V), a large pixel size (20×20μm^2) and a clock frequency of 5MHz. It was fabricated in a 0.35μm 2P3M CMOS technology.

Figure 16.7.4 shows the photoelectric conversion characteristics on the two vertical scales of the input-converted voltage for all the signals, and the digital signal for $S1$, $S2$ and Si. In the voltage readout operation, the rolling electrical shutter time is sequentially varied as 1/30s, 1/500s, 1/8ks and 1/130ks, shortening the exposure time by 1/16 between the respective steps. The voltage readout operation with 4 splits of the exposure time shows linear responses in the incident light ranging from about 10^{-2} to 10^{6}lx and extends the DR up to about 160dB. In addition, the current readout operation also realizes good photoelectric conversion characteristics from about 10^{5} to 10^{8}lx. The hybrid operation of the voltage and the current readouts is found to extend the DR over 200dB.

Figure 16.7.5 shows the sample images sequentially capturing four pictures of the voltage readout operation and one picture of the current readout operation. It is found that the image sensor is capable of capturing various scenes with the incident light ranging from about 10^{-2} to 10^{8}lx with the lens iris fixed.

Figure 16.7.6 shows the summary of the performance. Figure 16.7.7 is the chip micrograph, the chip size is 2.6×2.6mm^2.

References:

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[2] M. Loose, et al., "A Self-Calibrating Single-Chip CMOS Camera with Logarithmic Response," *IEEE J. Solid-State Circuits*, vol.36, pp.586-596, 2001.

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[4] S. Sugawa, et al., "A 100 dB Dynamic Range CMOS Image Sensor Using a Lateral Overflow Integration Capacitor," *ISSCC Dig. Tech. Papers*, pp.352-353, Feb., 2005.

[5] N. Akahane, et al., "A Sensitivity and Linearity Improvement of a 100 dB Dynamic Range CMOS Image Sensor Using a Lateral Overflow Integration Capacitor," *Symp. on VLSI Circuits*, pp.62-65, 2005.

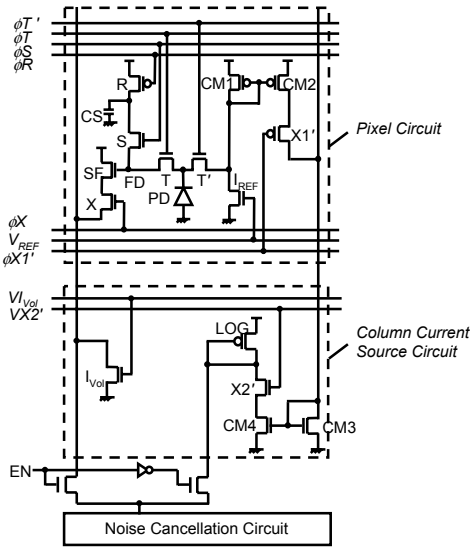

Figure 16.7.1: Schematic of a pixel.

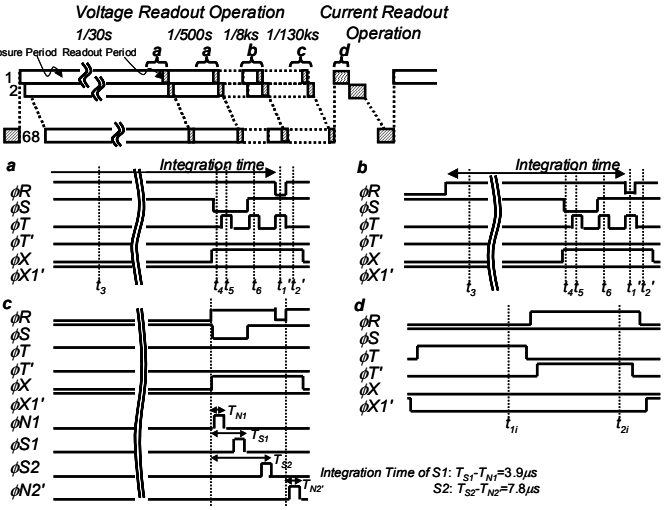

Figure 16.7.2: Timing diagram of the pixel operation.

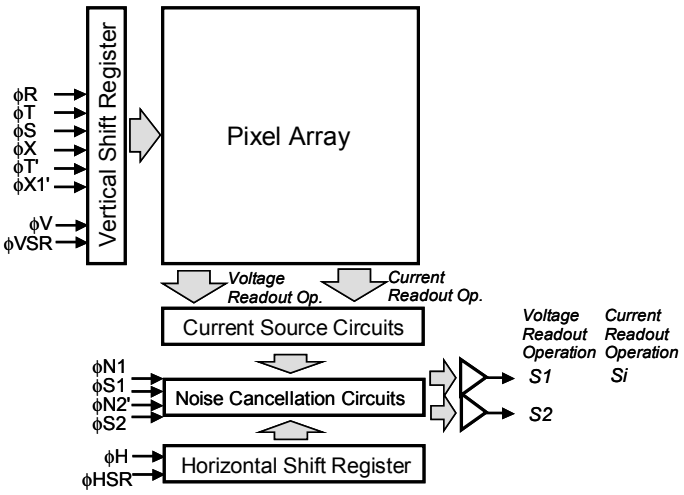

Figure 16.7.3: Block diagram of the image sensor.

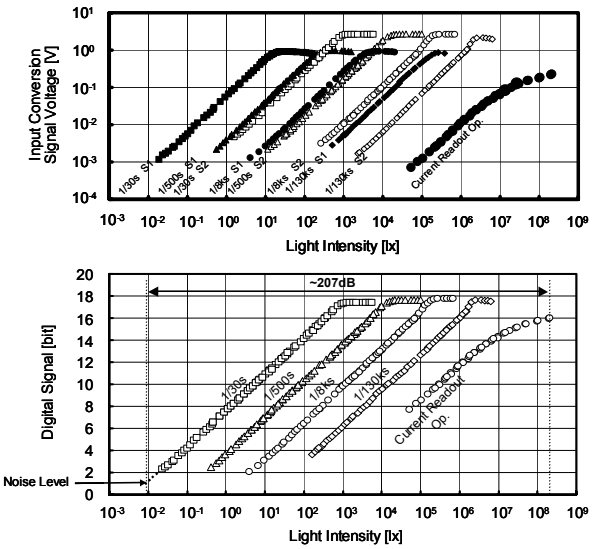

Figure 16.7.4: Photoelectric conversion characteristics.

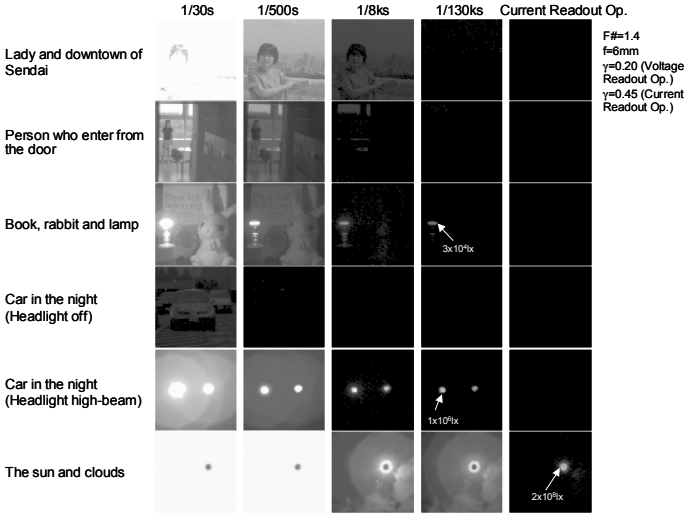

Figure 16.7.5: Sample images.

Chip Size			2.6 x 2.6 mm^2
Process technology			0.35μm 2P3M CMOS
Pixel size			20 × 20 μm^2
Number of pixels	Effective		64 × 64
	Total		70 × 68
Random noise (Input conversion noise)			0.30 mV$_{rms}$
FPN (Input conversion noise)			0.30 mV$_{rms}$
Dynamic Range	Voltage Readout Op.	1/30s	~ 100dB (9.0 × 10^{-3} – 9.3 × 10^2 lx)
		1/30s to 1/500s	~ 126dB (9.0 × 10^{-3} – 1.9 × 10^4 lx)
		1/30s to 1/8ks	~ 148dB (9.0 × 10^{-3} – 2.2 × 10^5 lx)
		1/30s to 1/130ks	~ 169dB (9.0 × 10^{-3} – 2.5 × 10^6 lx)
	Voltage Readout Op. & Current Readout Op.		~ 207dB (9.0 × 10^{-3} – 2.0 × 10^8 lx)

Figure 16.7.6: Performance summary.

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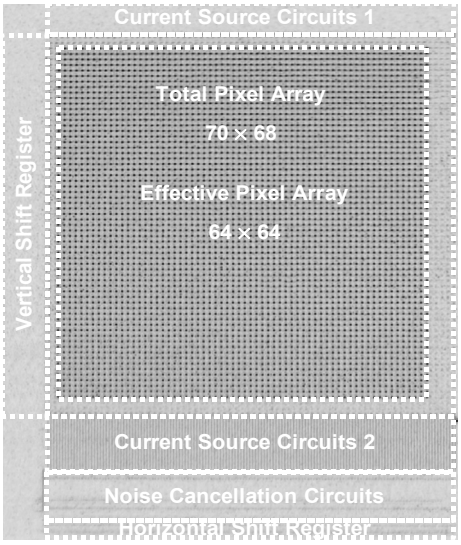

Figure 16.7.7: Chip micrograph.

